



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/650,890	08/28/2003	Tze-Chiang Chen	FIS920010295US2	8720
7590	08/16/2004		EXAMINER	
IBM, Corp. 2070 Route 52 B/300, Z482 Hopewell Junction, NY 12533			LEE, CALVIN	
			ART UNIT	PAPER NUMBER
			2825	

DATE MAILED: 08/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.



**OFFICE ACTION*****Claim Objection***

1. Claim 20 is objected to because of the following informality:

Claim 20 line 10, replace “dielectric” with --hardmask-- (to match with Figs. 2, 3 and disclosure).

***Claim Rejections - 35 U.S.C. § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 20, 27, 31, 33, and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by *Wang* (US 20020100907).

*Wang* discloses a method for forming an interconnect structure, comprising the steps of:

- depositing on a dielectric layer 18 a hardmask layer 26 of SiN, which has a top surface [Fig. 1]
- forming at least one opening in the dielectric layer [Fig. 3]
- depositing a conductive liner/barrier 20 in the opening
- filling the opening with copper material, thereby forming at least one conductor 22, 24, which has a surface coplanar with the top surface of the hardmask layer
- depositing a first material on the conductor, thereby forming a first cap layer 28 of SiN [pages 1-2]
- depositing a second material on the first cap layer, thereby forming a second cap layer 38 of SiC

***Claim Rejections - 35 U.S.C. § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 21-25 are rejected under 35 U.S.C. 103(a) as being anticipated by *Wang*, as applied to claim 20, in view of *APA* (*applicant's prior art*), and further in view of *Jang* (US 6,503,818).

*Wang* does not explicitly disclose such features as:

\* the first material is silicon nitride, and the HDP CVD process includes placing the substrate into a reactor chamber at a pressure of about 0.1 millitorr to about 50 millitorr and at a temperature of about 200°C to about 500°C, and exposing the substrate to at least one gas selected from the group consisting of silane, nitrogen, argon and helium; and

\*\* the second material is silicon nitride, and the PE CVD process includes placing the substrate into a reactor chamber at a pressure of about 0.1 torr to about 10 torr and a temperature of about 150°C to about 500°C, and exposing the substrate to at least one gas selected from the group consisting silane, ammonia, nitrogen and helium

*APA* suggests forming a cap layer by PECVD but preferably HDPCVD (has better adhesion)

Furthermore, a cap layer formed by HDPCVD (or PECVD) is known to the semiconductor processing art as evidenced by *Jang* disclosing a layer 18 of SiO or SiN formed by HDPCVD process in a reactor chamber at a pressure of about 1 to about 3 millitorr and at a temperature of about 350°C to about 400°C, and exposing the substrate to at least one gas selected from the group consisting of silane, argon and oxygen [Fig. 3].

It would have been obvious to one of ordinary skill to have modified the process of *Wang* by utilizing HDPCVD to form a first cap layer for the purpose of enhancing adhesion to the underlying layer [col. 6, ln.60].

7. Claim 26 is rejected under 35 U.S.C. 103(a) as being anticipated by *Wang*, as applied to claim 20, in view of *Ngo et al* (US 6,528,432).

*Wang* does not disclose performing a plasma pre-cleaning. Nevertheless, such plasma pre-cleaning is known to the semiconductor processing art as evidenced by *Ngo et al* disclosing subsequent to metal deposition the upper surface of an ILD is treated with plasma containing H prior to depositing the capping layer, wherein the plasma cleaning includes heating the substrate at a temperature of about 380 to 420°C for a time of about 15 to 35 seconds [col. 4].

It would have been obvious to one of ordinary skill to have modified the process of *Wang* by utilizing a plasma pre-cleaning for the purpose of solving degradation problems attendant upon employing organic carbon-containing low-k materials for ILD [col. 3].

8. Claims 28-30 are rejected under 35 U.S.C. 103(a) as being anticipated by *Wang* in view of *applicant's prior art* or *Ngo et al (US 6,528,432)*.

a) In re claim 28, *Wang* does not disclose an adhesion promoter layer. Nevertheless, such adhesion promoter layer is known to the semiconductor processing art as evidenced by *APA* disclosing [Fig. 1] an adhesion promoter 11 on a substrate 10.

It would have been obvious to one of ordinary skill to have modified the process of *Wang* by utilizing an adhesion layer for the purpose of promoting an adhesion between the substrate and the overlying interconnect structure.

b) In re claims 29-30, *Wang* does not disclose that the dielectric layer is formed of an organic thermoset polymer having a dielectric constant of about 1.8 to about 3.5. *APA* [page 3] discloses dielectric layers 12 and 19 made of a low-k polymeric thermoset material. Moreover, *Ngo et al* also suggests other low-k ( $\approx 3$ ) dielectrics including various poly(arylene)ethers, etc.

It would have been obvious to one of ordinary skill to have modified the dielectric layer of *Wang* by utilizing a polymer dielectric layer (whose dielectric constant is much lower) for advanced interconnect structure with a lower capacitance.

9. Claims 32 and 34-36 are rejected under 35 U.S.C. 103(a) as being anticipated by *Wang* in view of *Ngo et al (US 6,593,237)*.

*Wang* is silent about the composition of the first and second cap layers. *Ngo et al* suggests a stop layer of SiN with a hydrogen concentration above atomic %" [col. 4]. However, *Ngo et al* does not explicitly disclose the claimed amount of silicon, nitrogen (or carbide), and hydrogen in the composition of the cap layers.

It would have been an obvious to one having ordinary skill in the art to have modified the cap layers of *Wang* by utilizing the claimed composition because one would adjust either the concentration ratio or the atomic amount of depositing materials (i.e., silicon, nitrogen, and hydrogen) to result in the most effective cap layers.

10. Claims 38-39 are rejected under 35 U.S.C. 103(a) as being anticipated by *Wang* in view of *Lage et al* (US 6,184,073).

*Wang* does not disclose the cap layer comprising a plurality of thin films. Nevertheless, such multi-layer capping is known to the semiconductor processing art as evidenced by *Lage et al* disclosing an oxide (or nitride) capping layer including a plurality of films [col. 4]

It would have been obvious to one of ordinary skill to have modified the process of *Wang* by utilizing a cap layer with plurality of films for the purpose of obtaining a better cap layer having a desired thickness and/or variety of the layer materials.

***Contact Information***

11. Any inquiry concerning this communication from the Examiner should be directed to *Calvin Lee* at (571) 272-1896, Monday to Thursday, from 7 to 5 (ET). If attempts to reach the examiner by telephone are unsuccessful, Art Unit 2825's Supervisory Patent Examiner *Matthew Smith* whose telephone number is (571) 272-1907.

Any inquiry relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0596. The fax phones are (703) 872-9318 for regular communications and (703) 872-9319 for After-Final communications.

CL

August 2, 2004

  
CARIDAD EVERHART  
PRIMARY EXAMINER